REMARKS

Claims 1-12 were pending in this application. By the above amendment, claim 2 has been cancelled and claims 13 and 14 have been added.

The Office Action dated June 13, 2005, has been received and carefully reviewed. In that Office Action, claims 2 and 7-8 were objected to as being in improper dependent form. In addition, claims 1-5, 7, 9 and 11 were rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuishi in view of Shimatani, and claims 6, 8, 10 and 12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuishi and Shimatani and further in view of McGarvey. Because it is believed that the claimed invention is not shown or suggested by the art of record, reconsideration and allowance of claims 1 and 2-14 is respectfully requested.

CLAIM OBJECTIONS

Claim 2 was objected to for being in improper dependent form. By the above amendment, claim 2 has been replaced by claim 13, and claim 7 has been amended to depend from claim 13. It is believed that these amendments obviate the claim objection.

OBVIOUSNESS REJECTIONS

Claim 1 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuishi in view of Shimatani. Claim 1 requires a data processing system that includes, *inter alia*, an arbitration controller for determining, based on first and second bus use permission requests from a data transfer controller and a central processing unit signals, which of these units should obtain a permission to use a system bus. Claim 1 further requires a section for setting a first data amount which can be continuously transferred by at least one function module connected to the data transfer controller. The Office Action acknowledges that Mitsuishi does not disclose a section for setting a first data amount as claimed. However, Shimatani is cited to show a system in which the number of data to be transferred by one DMA transfer can be set.

First, it is noted that a proper motivation for combining these references has not been provided and that therefore a *prima facie* case of obviousness has not been presented. Moreover, even if a motivation for combining these references is provided, it is respectfully submitted that

the result would not be the invention required by claim 1.

The Office Action argues that it would have been obvious to use Shimatani's mechanism for designated the number of data to be transferred by one DMA as "a mechanism for specifying the amount of data to be transferred." It is respectfully submitted that this is a tautological statement – it is merely a restatement of the purpose of Shimatani's element. The statement does not identify a motivation or reason for adding Shimatani's element to Mitsuishi's device.

The Office Action also argues that it would have been obvious to add Shimatani's "suspending means" to Mitsuishi to "prevent contention of the system bus." However, Mitsuishi teaches that a DTC relinquishes bus use at halting points between operating steps, column 18, lines 23-24. Mitsuishi discloses a system where contention for a system bus does not appear to be a problem; therefore, Mitsuishi provides no motivation for addressing this non-existent problem by using the disclosure of Shimatani. Moreover, Shimatani's "release period" is a period during which the CPU must relinquish control of a bus. This teaching would not motivate one to provide a period during which the DMA generally cannot access the bus as recited in claim 1. Because the Office Action does not identify a proper motivation for combining Mitsuishi and Shimatani, it is respectfully submitted that a *prima facie* case of obviousness has not been presented and that claim 1 patentably distinguishes over the references of record.

Even if the references were combined, the result would not be the invention required by claim 1. As discussed above, Shimatani teaches providing a release period during which a CPU must release a bus so that a DMA controller can use a bus. Shimatani does not suggest a section for suspending an output of the first [DMA] bus use permission request signal to the arbitration controller for at least one clock cycle after a data transfer by the at least one function module is completed. Therefore combining Mitsuishi and Shimatani would at most suggest that a CPU should relinquish control of a bus for some period of time. The combination does not suggest a period during which the DMA generally cannot use the bus as claimed. For this reason as well, claim 1 is submitted to be allowable over the art of record.

Claims 3-6 and 9-12 depend from claim 1 and are submitted to be allowable for the same reasons as claim 1.

Claim 3 further distinguishes over the references of record by requiring that, after a data

transfer is completed and the output of the first bus use permission request signal is suspended for at least one clock cycle, if the output of the first bus use permission request signal to the arbitration controller is further suspended for another one or more clock cycles, the permission to use the system bus is given to the central processing unit based on the second bus use permission request signal. The Office Action takes Official Notice of the fact that, when one device is prevented from requesting permission to use a bus, another device is given permission use the bus. It is submitted that this statement about the operation of bus systems is not capable of such "instant and unquestionable demonstration as to defy dispute," *In re Ahlert*, 165 U.S.P.Q. 418, 420 (CCPA 1970); MPEP 2144.03, as is required to support the use of Official Notice. There may be times, for example, when no device is given permission to use a bus, or, alternately, when a device uses the bus without permission. It is therefore respectfully requested that the examiner produce documentary evidence in the next Office Action to support this finding. Claim 3 is submitted to be allowable.

Claim 4 further distinguishes over the references of record by requiring a section for setting a second data amount which can be continuously transferred by a central processing unit. The Office Action acknowledges that this is not shown in the prior art, but indicates that it would have been obvious to provide such a section. No statement explaining why one skilled in the art would be motivated to add such a section to Mitsuishi or Shimatani is provided and therefore a *prima facie* case of obviousness has not been presented. The fact that Mitsuishi does not give permission to a DTC until a CPU is finished does not in any manner suggest a section for setting a second data amount as claimed. Claim 4 is submitted to further distinguish over the art of record for this reason.

Claims 6, 8, 10 and 12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuishi and Shimatani and further in view of McGarvey. Claims 6, 8, and 12 depend from claim 1. McGarvey does not address the shortcomings of Mitsuishi and Shimatani discussed above in connection with claim 1. Claims 6, 8 and 12 are therefore submitted to be allowable for the same reasons as claim 1. Claim 10 depends from claim 13 and is submitted to be allowable for the same reasons (provided hereafter) as claim 13.

McGarvey discloses a digital camera having a controller processor 28 for producing

clock signals, receiving user input from a shutter release and initiating a capture sequence. McGarvey is silent as to granting permissions to use a data bus and transferring data by DMA. If the Office Action is suggesting that the control processor of McGarvey be replaced with the DMA controller of Shimatani or the data transfer controller of Mitsuishi, it is respectfully submitted that the resulting device would be non-functional. The "controllers" of Mitsuishi and Shimatani do not perform the same functions as the control processor of McGarvey and therefore could not replace McGarvey's control processor. Moreover, nothing in the McGarvey reference discloses the type of bus system used or the type of bus controller used, if any. Therefore, nothing in the references of record suggest that the McGarvey device would be improved if one of the Mitsuishi of Shimatani devices were somehow combined therewith. Claims 6, 8 and 12 are submitted to further distinguish over the art of record for this reason.

New claim 13 is also submitted to be allowable. Claim 13 requires a data processing system that includes, *inter alia*, a first section for setting a first data amount which can be continuously transferred by a at least one function module, a second section for selectively suspending an output of a first bus use permission request signal to an arbitration controller for at least one clock cycle after a data transfer by the at least one function module is completed unless a data transfer request signal is being issued by at least one function module and the priority of the at least one function module issuing the request is higher than a priority of the central processing unit; and a third second for giving the permission to use the system bus to one of the data transfer controller and the central processing unit in such a manner that the data transfer controller has a priority over the central processing unit during a period when the first bus use permission request signal is being issued. Mitsuishi suggests that a DTC relinquish use of a bus from time to time, but provides no suggestion that an output of a first bus use permission request signal should be selectively suspended unless a data transfer request signal having a higher priority than a priority of a CPU is being issued. Claim 13 and its dependent claims 7 and 8 are submitted to be allowable for at least this reason.

Claim 14 is also submitted to be allowable over the art of record. Claim 14 requires a method of processing data that includes connecting at least one function module to a single system bus, providing a data transfer controller, outputting a data transfer request signal from the

at least one function module to the data transfer controller, providing an arbitration controller, outputting from the data transfer controller to the arbitration controller a first bus use permission request signal based on the data transfer request signal output from the at least one function module, connecting a central processing unit to the system bus, outputting a second bus use permission request signal from the central processing unit to the arbitration controller, determining, based on the first and second bus use permission request signals, which of the data transfer controller and the central processing unit should obtain a permission to use the system bus, setting a first data amount which can be continuously transferred by the at least one function module, suspending the first bus use permission request signal to the arbitration controller for at least one clock cycle after a data transfer by the at least one function module is completed, and giving the permission to use the system bus to one of the data transfer controller and the central processing unit in such a manner that the data transfer controller has a priority over the central processing unit during a period when the first bus use permission request signal is being issued. The references of record do not show or suggest a method including these steps. The arguments presented above in connection with claim 1 are also relevant to the patentability of this claim. Claim 14 is submitted to be allowable over the art of record for at least these reasons.

CONCLUSION

Each issue raised in the Office Action dated June 13, 2005, has been addressed, and it is believed that claims 1 and 3-14 are in condition for allowance. Wherefore, reconsideration and allowance of claims 1 and 3-12 and examination of claims 13 and 14 is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Scott Wakeman (Reg. No. 37,750) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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AMENDMENTS TO THE DRAWINGS

The attached drawings have been modified by adding the legend "conventional art" to Figures 12, 13 and 14.